A BIST Scheme for RF Power Amplifiers

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Abstract

One can find today system-on-chip devices comprising also radio-frequency blocks. These highly integrated circuits raise extraordinary challenges for testing, jeopardizing the low cost requirements associated often to these products. A built-in self test scheme for RF power amplifiers based on a polynomial fitting approach is proposed here, which takes advantage of the existing local oscillator, up-conversion mixer, and pre-driver, allowing for low area overhead and performance degradation. Simulation and experimental results for gain and linearity (1 dB compression and third order interception points) obtained with a GaAs distributed amplifier are presented which confirm the validity of the method. The BIST scheme proposed for implementing this method on-chip is then described, together with preliminary simulation results.

1. Introduction

The progress attained with submicron CMOS technologies allows today not only to fully integrate RF transceivers on a single silicon substrate, but also to integrate these with the baseband (BB) processing and user interface functions [10, 1]. With the capability and benefits of monolithic integration being now extended to RF circuits, the accessibility to test nodes for control and observation is becoming more and more difficult as generating, propagating, and measuring high frequency signals is more acute [2].

Figure 1 shows a typical set-up to perform single tone or two tone measurements. Besides the RF signal generators, bias sources, and measurement instruments, impedance matching couplers and attenuators are required to interface the different devices. In the two tone case an impedance matching and combiner (IM/C) coupler is required to add the two signals and avoid interaction between the two RF generators. New test procedures are then required to avoid the necessity for complex and delicate set-ups and which allow testing embedded RF circuits.

This issue has deserved the attention from the research community and different solutions have already been published [9, 5, 11, 8, 3]. These works have addressed mainly Low Noise Amplifiers, or the transmitter and receiver subsystems as a whole making it difficult to diagnose defective RF macros. In particular, the test of power amplifiers (PAs) has not been addressed with the same effort.

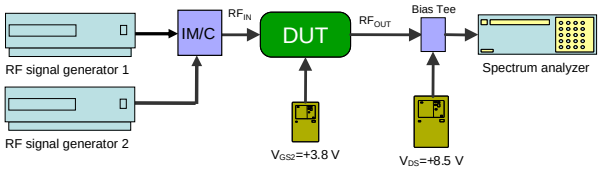


Figure 1. Typical RF power amplifier test set-up.

PAs are usually tested for linearity, output power, gain, and power added efficiency (PAE) using a single tone stimulus. Two-tone or more complex digital modulated signals are used to measure parameters such as intermodulation distortion (IMD) and adjacent channel leakage power ratio (ACPR). However, at the production stage typical tests include gain, output power, P_{1dB}, and input return loss. In [12] a PA test methodology based in the analysis of the transient response of the PA's dynamic power supply current (i_{DD}) is proposed for faster production test. Parameters such as gain and PAE are estimated after the i_{DD} signature using non-linear regression functions computed using multivariate adaptive regression splines. The amplifier under test parameters are estimated by using these regression function to map the observed transient current to the corresponding specifications. The method requires then testing a number of known good devices to provide the mapping regression functions.

In this paper a method to test for power and linearity, after the estimation of 1 dB compression (P_{1dB}) and 3rd order input interception (IIP3) points is presented, which is suitable to be built on-chip. The performed measurements provide directly an estimation of these parameters. Simulation and experimental results obtained with a GaAs distributed amplifier are shown which confirm the validity of the method. Concerning on chip implementation, as a single tone stimulus is employed, the existing local oscillator can be used as stimulus generator. To propagate this stimulus into the PA, instead of creating an alternative path using additional switches (which could degrade performance), a reconfigurable up-conversion mixer is used to route the stimulus to the PA input. Advantage is also taken of the existing variable gain PA driver to control the amplitude of the stimulus at the PA's input. Simple diode based power detectors are used to obtain DC measures of the PA's input and output powers. These measures are then used off-chip to compute the polynomial that best fits the PA's

gain characteristic, whose coefficients allow us to obtain P_{1dB} and IP3. As only DC and digital control signals are needed to be interchanged with the tester, general purpose test infrastructures can be used for control and observation purposes.

Next section reviews the mathematics behind the computation of P_{1dB} and IP3 values after the polynomial fitting coefficients. Section 3 presents simulation and experimental results obtained with a GaAs distributed amplifier. Section 4 describes the implementation of the method on chip, and presents simulation results obtained with the IC prototype being designed. Finally, section 5 highlight the main conclusions.

2. Polynomial-Fitting Testing Method

The output response of an amplifier with weak non-linear behaviour can be modelled as a Taylor series in terms of the input voltage:

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + ... \quad (1)$$

The Taylor series model is valid for memoryless non-linear functions, while Volterra series are required when memory effects have to be included. Nevertheless, the Taylor series model is applicable when the number of stages is small.

If a single frequency signal $v_{in} = Acos(\omega t)$ is applied at the input, the output voltage becomes

$$\begin{aligned} v_{out} &= a_0 + a_1 A cos(\omega t) + a_2 A^2 cos^2(\omega t) + \\ &\quad a_3 A^3 cos^3(\omega t) + ... = \\ &= (a_0 + \frac{1}{2} a_2 A^2) + (a_1 A + \frac{3}{4} a_3 A^3) cos(\omega t) \\ &\quad + \frac{1}{2} a_2 A^2 cos(2\omega t) + \frac{1}{4} a_3 A^3 cos(3\omega t) + ... \end{aligned} \quad (2)$$

The voltage gain at frequency ω_0, retaining only terms up to the third order, can be found from

$$G_v = \frac{v_{out}(\omega_0)}{v_{in}(\omega_0)} = \frac{a_1 A + \frac{3}{4} a_3 A^3}{A} = a_1 + \frac{3}{4} a_3 A^2 \quad (3)$$

The 1 dB compression point, which characterizes the occurring AM/AM distortion, is defined as the power level at which the output power decreases 1 dB from the ideal characteristic. That is,

$$\begin{aligned} P_{real} &= P_{ideal} - 1dB \\ 10log[\frac{1}{2}\frac{(a_1 A + \frac{3}{4} a_3 A^3)^2}{Z}] &= 10log[\frac{1}{2}\frac{a_1^2 A^2}{Z}] - 1dB \end{aligned} \quad (4)$$

which yields,

$$A_{1dB} = \sqrt{|(\frac{a_1}{10^{\frac{1}{20}}} - a_1)\frac{4}{3a_3}|} \quad (5)$$

for the input voltage at the 1 dB compression point.

If a two-tone input voltage, consisting of two closely spaced frequencies, $v_{in} = A(cos(\omega_1 t) + cos(\omega_2 t))$, is applied the amplifier non-linearity gives place to intermodulation products of order $|m| + |n|$, i. e., harmonics of the form $m\omega_1 + n\omega_2$, with $m, n = 0, \pm 1, \pm 2, \pm 3, ...$ The third order intercept point can be defined as the input (or output) for which the power of the third order intermodulation components is equal to the power of the first order (ideal response) component. One can express the input- and output-referred third-order intercept point powers, using the polynomial coefficients as, respectively,

$$\begin{aligned} IIP_3 &= \frac{1}{2}\frac{4a_1}{3a_3 \times Z_{in}} \\ OIP_3 &= P_{o\omega_1|P_i=IIP3} = \frac{1}{2} a_1^2 \frac{4a_1}{3a_3}\frac{1}{Z_{out}} = \frac{2a_1^3}{3a_3 Z_{out}} \end{aligned} \quad (6)$$

These equalities lead us to define a test method to measure P_{1dB} and IP3 based on obtaining the polynomial that best fits the amplifier's transfer characteristic. This can be done by sweeping the PA's input voltage, and measuring the respective output levels. From the resulting set of input/output values one can find the best fitting polynomial whose coefficients (a_1 and a_3) allow us to calculate the corresponding P_{1dB} and IP3 values.

3. Simulation and experimental results

To evaluate the applicability of this testing approach to power amplifiers, simulation and experimental results were obtained using a GaAs distributed power amplifier [6]. The simplified topology of this amplifier, which comprises 6 cascode cells in cascade, is shown in figure 2. Its ADS model was used to obtain simulation results, and a prototype fabricated with a 150 nm GaAs power pHEMT technology from United Monolithic Semiconductors (figure 3) was used to confirm these results experimentally. Figure 4 shows the input/output power characteristic obtained by simulation.

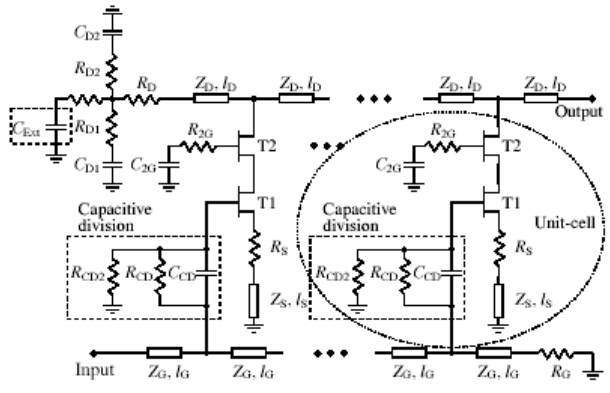


Figure 2. Schematic of GaAs distributed PA (DC a 20GHz).

A sequence of 16 equally spaced voltage levels was applied and the resulting output values registered. This set of 16 coordinates was used to obtain the respective best fitting

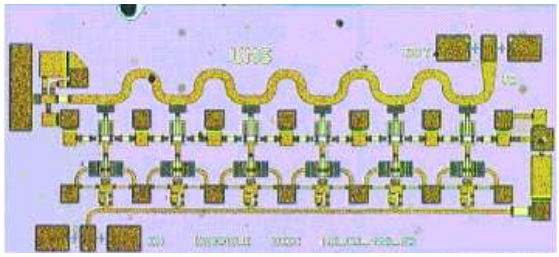


Figure 3. Photo of GaAs distributed PA prototype.

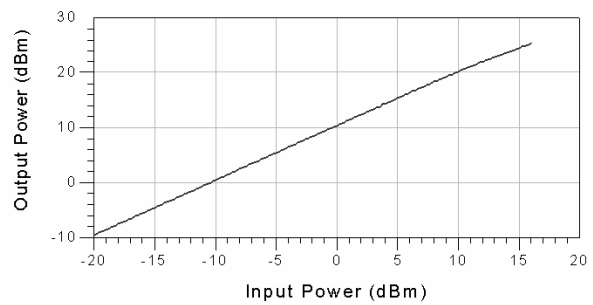


Figure 4. PA's power I/O characteristic at 20 GHz.

third-order polynomial, as shown in figure 5. This operation was repeated at different frequencies, and in each case the P_{1dB} values given by ADS, compared with those obtained using the coefficients of the best fitting polynomial. A close agreement between these results was confirmed as it is shown in figure 6, which shows input- and output- referred P_{1dB} points obtained with ADS (curve A in red) and with the polynomial fitting method (curve B in blue). In all the five cases the differences are very small. Larger differences were obtained for the IP3 point as it can be seen in figure 7. However, the differences between the expected values given by the ADS simulation (curve A in red) and those obtained with the fitting polynomial (curve B in blue) do not differ more than 1 dB.

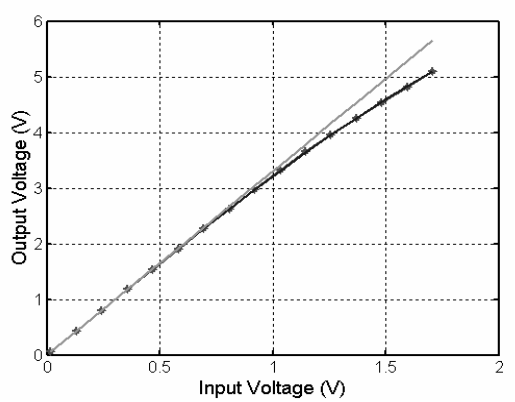


Figure 5. Set of points that define the $V_{out}vsV_{in}$ characteristic, and the respective best fitting 3rd order polynomial.

Experimental results were then obtained with the fabricated prototype using a single tone stimulus set-up to measure P_{1dB} and a dual tone stimulus set-up to measure IP3.

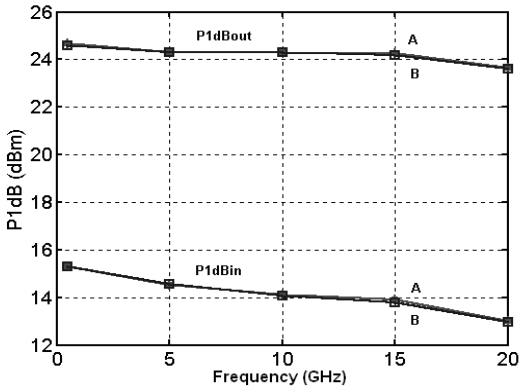


Figure 6. PA's P_{1dB} variation with frequency. Curve A - ADS simulation; curve B - polynomial fitting.

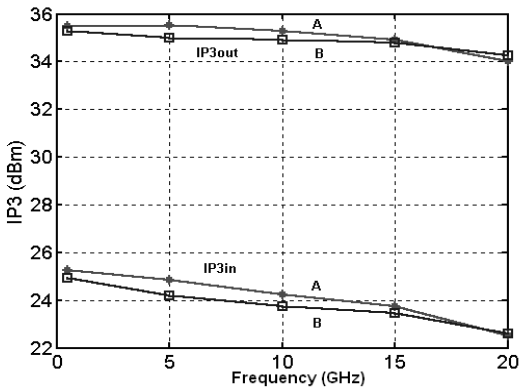


Figure 7. PA's IP3 variation with frequency. Curve A - ADS simulation; curve B - polynomial fitting.

Table 3 summarises these results, together with those obtained using the polynomial fitting method (in both cases these are output referred values). One can see that a very close agreement was found again.

Other simulation and experimental results where obtained with class A amplifiers which showed the same good agreement between the values obtained with the traditional measurement procedure and with the polynomial fitting approach.

4. On-chip Implementation

Considering the relative simplicity of the polynomial fitting method, both in terms of the required implementation resources and computational effort, one finds it suitable for

Table 1. Experimental results obtained using the classical procedures and polynomial fitting.

Frequency	Measured		Polynomial fit	
(GHz)	P_{1dB}	OIP3	P_{1dB}	OIP3
10	20.835	32.585	20.980	31.287
15	20.420	31.090	20.540	31.428
20	18.920	30.330	18.950	29.975

on-chip implementation. All that is necessary is the capability to sweep the PA's input voltage in a range covering from about $A_{1dB}/10$ to $1.5 * A_{1dB}$ provided the amplifier does not enter into deep saturation, and to measure the corresponding output voltage levels. In order to minimize test circuitry overhead and performance degradation, one should take advantage of existing resources whenever that is possible.

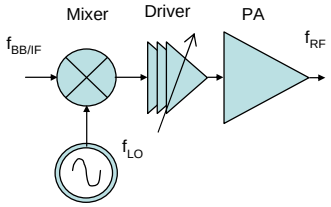


Figure 8. Typical topology of an emitter front-end.

Figure 8 shows the typical topology of an RF emitter front-end. It includes a mixer to up-convert the BB or intermediate frequency (IF) signals to the RF transmitting frequency that results from the sum (or difference) of the local oscillator (LO) and the BB/IF frequencies. The PA is often preceded by a driver (pre-amplifier) which provides also a means to control PA's output power. Two methods of power control are commonly used: PA's input swing control using a variable gain amplifier (VGA), and variable bias control. Other approaches based on digitally controlled output drivers have also been proposed [10, 13, 4]. These are based on switching on/off an array of, typically three to five, binary area-weighted transistors, providing thus a discrete control of the PA dynamic range.

Taking advantage of this topology one can use the LO as stimulus generator and the driver's power control feature to provide the required PA's input voltage sweep. To avoid the inclusion of extra switches to shift the driver's input from the up-conversion mixer output to the LO, one has to be able to generate a single-tone continuous waveform (CW) at the mixer's output. This requires a reconfiguration of the mixer's operation in order that, in test mode, it propagates the single-frequency LO's signal without being modulated by the BB/IF one. Alternatively a specific signal can be injected from the BB interface avoiding thus any modifications in the mixer. Nevertheless, using a reconfigurable mixer just a simple digital signal can be used to switch between normal mission and test operating modes. Furthermore, using AC/DC converters as power detectors, the entire test operation can be accomplished without the need to generate, capture or propagate any high frequency signals, and low frequency buses can be used to control and capture the DC detectors' outputs.

4.1. IC prototype

An IC prototype is being designed to implement this test methodology. It comprises the blocks depicted in figure 8, as well as the detectors to be used to obtain the PA's input/output transfer characteristic. Figure 10 shows the PA scheme together with the controllable driver [4]. The driver comprises four sets of two transistors. The top transistors of three of them are switched on/off with controlling bits (C_0 — C_2). The widths of the bottom ones are weighted in order to obtain eight different equally spaced voltage levels spanning the PA's input range. Figure 9 shows the gain obtained with the driver in the highest gain (C_0=C_1=C_2=1) mode. The 1 dB compression point measured in this case is P_{1dB}=8.1 dBm.

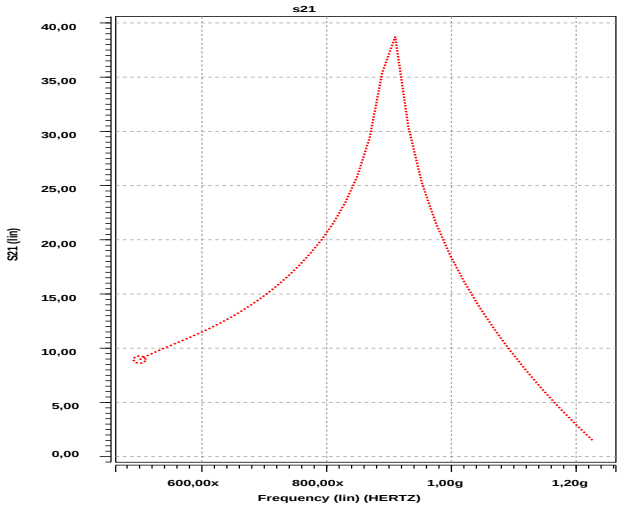


Figure 9. Driver and PA's gain.

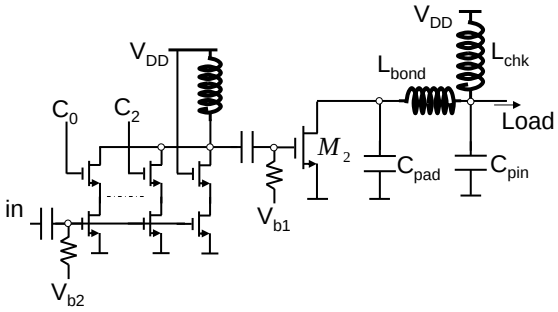


Figure 10. Power amplifier with controllable pre-amplifier.

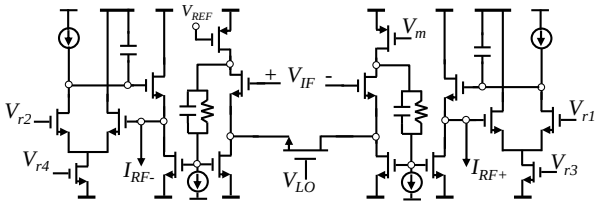
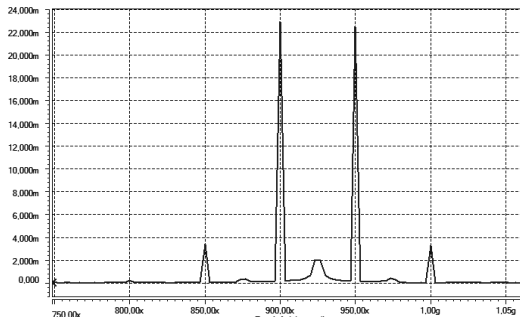


Figure 11. Up-conversion mixer.

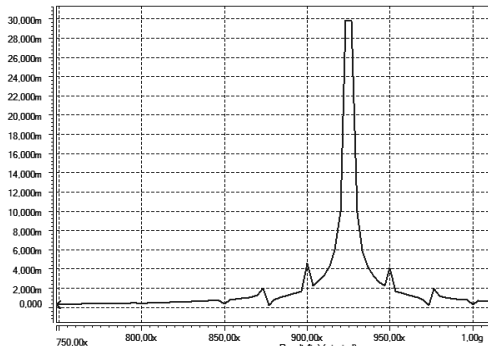
Figure 11 shows the up-conversion mixer. This mixer was adopted from [7] and modified in order to support both normal mission and test modes. In normal mission mode node V_m is connected to V_{REF} allowing the two sides of the mixer to operate simetrically, generating a differential

output current. Due to the differential operation the V_{LO} frequency component is suppressed in the mixer's output. In test mode V_{IF} is disconnected and V_m is pulled up to V_{DD}, leading the mixer's right side to be off and the output signal to be of constant amplitude at the LO frequency. A differential to single-ended signal converter provides the interface between the mixer output and the driver input.

Figures **??**.a) and **??**.b) show the PA's output spectrum, respectively, in normal mode and in test mode when a single tone signal is present at the V_{IF} input. In normal mode two main frequencies at $f_{LO} \pm f_{IF}$ are generated, while in test mode one can see mainly a tone at f_{LO}.



(a)



(b)

Figure 12. PA's output spectrum: a) normal mode; b) test mode.

Using the proposed reconfigurable mixer the required extra circuitry overhead corresponds to a transmission gate used to switch-off the mixer's V_{IF} input plus the two detectors. Their presence imply a degradation of about 1 dB in the gain seen between the V_{IF} input and the PA output.

The detectors (figure 13) to be placed at the PA's input and output (the driver's gain is excluded in the test operation) allow to obtain the different voltage coordinates which define the PA's input/output characteristic. The detectors' characteristic shown in figure 13 show that a good measure linearity is ensured. That is a critical requirement in order that the PA's characteristic linearity is not affected by the measures non-linearity.

4.2. Prototype simulation results

Figure 14 shows the voltage (rms values) transfer characteristics obtained observing the PA's input and output voltages, respectively, the expected one (solid red line) and that obtained using the power detectors' values (dashed

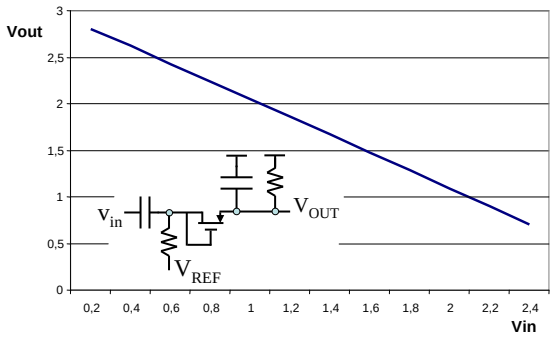


Figure 13. Power detector.

blue line). One can see that the last one follows the expected observed values with an error smaller than 0.1 dB. Figure 15 shows the respective power curves.

After finding the coefficients of the polynomials which define the two voltage curves one can compute the PA's P_{1dB} and IIP3 points using equations 5 and 6. Using the directly observed voltages the values P_{1dB}=7.2 dBm and IIP3=16.8 dBm are obtained. These values are slightly different from the ones mentioned above for the highest gain configuration, due to the non-linearity introduced by using the different stages of the driver to generate the sweep. Using the values provided by the detectors one obtains P_{1dB}=6.3 dBm and IIP3=16 dBm. The error due to using these simple AC/DC converters as power detectors is thus about 1.0 dB. Values were also obtained affecting the observed voltages with a random noise. With a peak noise amplitude equal to 1% the maximum voltage, one obtains for P_{1dB} a mean value of 6.5 dBm and a standard deviation of 0.9 dBm. For the IIP3 these values are 16.1 $\pm$ 0.9 dBm. Increasing the peak noise amplitude to 3% the maximum voltage, one obtains P_{1dB}=7.5 $\pm$ 3.7 dBm and IIP3=17.1 $\pm$ 3.8 dBm.

Concerning fault detection, taking the curve obtained with the detectors as a reference, it is also possible to know whether a fault is located in the PA or in the previous blocks, by mapping both input and output observed values with the reference ones. That is, if the observed input values match the expected ones and those at the output do not, a fault is detected in the PA. If the observed input values do not match the expected ones the fault is occurring before the PA. Placing more detectors allows to increase fault diagnosability.

5. Conclusions

A methodology is proposed which allows testing an embedded PA using a polynomial fitting characterization method. This method relies on applying a set of voltage values spanning the PA's dynamic range and on capturing the respective output values. From this set of input/output values one can obtain the polynomial that best fits the PA's transfer characteristic, whose coefficients allow one to calculate 1 dB compression and third order intercept point values. Simulated and experimental results have been ob-

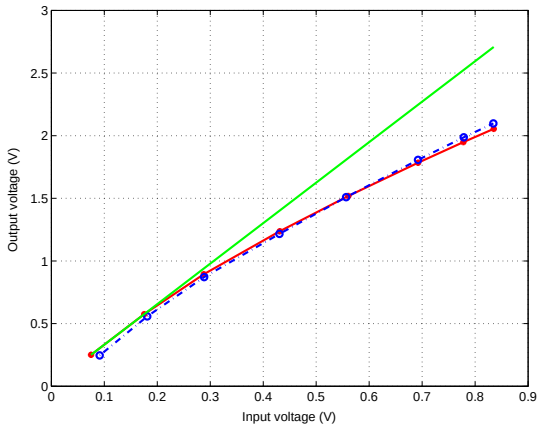


Figure 14. PA's voltage transfer characteristic.

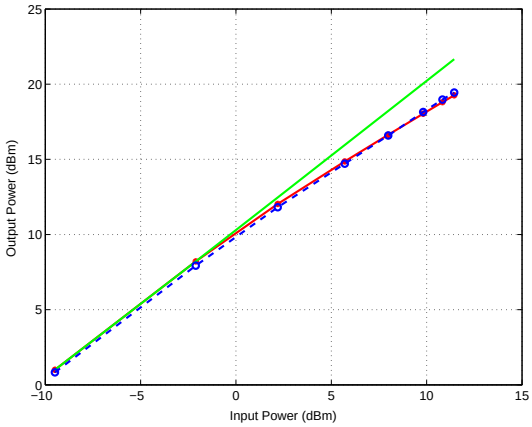


Figure 15. PA's power transfer characteristic.

tained which confirm the feasibility of this methodology to obtain accurate results for these parameters.

The BIST scheme being proposed to implement this method on-chip reuses the existing oscillator, up-conversion mixer, and PA's driver to generate the different amplitude stimuli. Simple diode based AC/DC converters are used as peak voltage detectors at the PA's input and output. The up-conversion mixer is modified in order to allow applying a single-tone stimulus at the PA's input, being the voltage sweep obtained using the scaling feature provided by the PA's driver. This avoids including extra circuitry for stimuli generation and propagation. The only extra circuitry that is required is a transmission gate required to switch-off the mixer's IF input and the two detectors. Simulation results show that a small performance degradation is obtained, and that parameters' values can be obtained with an error of about 1 dBm. As the test operation is controlled digitally and DC voltages are measured, no wide-bandwidth buses and specific instruments are required to deal with delicate high frequency signals.

Acknowledgment

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